ITL.0685US
(P13044)

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: LOWER PROFILE PACKAGE WITH POWER SUPPLY IN PACKAGE

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Express Mail No. EL857974099US

Date: January 2, 2002

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Background

This invention relates generally to integrated circuits and particularly to designs for packaging an integrated circuit die.

An integrated circuit chip may be fabricated on a substrate, which may be a silicon wafer, by microelectronic processing. Typically, a multiplicity of chips (dice), separated by scribe lines, is formed simultaneously on a single wafer. Individual dice or chips are separated by dicing or sawing on the scribe lines.

Individual dice need to be electrically coupled to external circuitry. However, the dice are fragile and too small to handle easily. Further, they may also be vulnerable to contamination and corrosion by the environment, and subject to overheating during operation unless heat is dissipated. A die package provides the die with mechanical support, electrical connections, protection from contamination and corrosion, and heat dissipation during operation.

The process of packaging the die may include attachment of the die to the package, the bonding of wires from leads on the package to pads on the die, and encapsulation of the die for protection.

A Power Supply In Package (PSIP) design replaces capacitive charge pumps in a die with inductive charge pumps located outside the die, but still within the same package with the die. The resulting reduced die sizes reduce fabrication costs.

The external inductive charge pump includes discrete passive circuit elements such as inductors and capacitors that are included within the package with the die. As a result of the lack of integration of the charge pump into the die, the resulting package is generally larger. Thus, cost savings may be achieved, but the price may be larger package sizes.

The larger package size may be a problem in some applications. Designers may be hesitant to use PSIP parts because doing so may require re-design of the board layout to accommodate the larger package size. In some cases, extra board real estate may be difficult to come by.

Thus, there is a need for PSIP packages that substantially preserve non-PSIP form factors.

Brief Description of the Drawings

Figure 1 is an enlarged cross-sectional view of a package for an integrated circuit in accordance with one embodiment of the present invention;

Figure 2 is an enlarged cross-sectional view of a package for an integrated circuit in accordance with another embodiment of the present invention; and

Figure 3 is a bottom plan view of the embodiment shown in Figure 2.

Detailed Description

Referring to Figure 1, a ball grid array (BGA) package 10 in accordance with one embodiment of the present invention may include a substrate 12 that may be electrically coupled to external circuitry using a multiplicity of solder balls 25. The package 10 may contain an integrated circuit die 14 attached to the substrate 12, for example using a suitable adhesive 18. In one embodiment, a set of low profile passive components 16a and 16b form a charge pump located externally of the die 14. The components 16a and 16b may be attached to the upper surface of the die 14, for example using the adhesive 18.

The charge pump components 16 may include inductors and capacitors. The adhesive 18 may be an epoxy adhesive. Further, since the charge pump components 16 are located in the package 10, albeit outside the die 14, the package may be Power Supply In Package (PSIP).

Wirebonds 20 provide electrical connections between the substrate 12 and the die 14 as well as between the substrate 12 and the passive components 16. A protective encapsulation 24 encapsulates the die 14 and components 16, forming a molded array package (MAP).

By using PSIP, a smaller die 14 size may be achieved. However, conventionally the package 10 size would exceed

the form factor of a non-PSIP package including generally the same electrical devices because of the lack of integration of the components 16.

The package 10 may substantially maintain the form factor of a corresponding non-PSIP package so that the package 10 may fit within the space allocated on boards for corresponding non-PSIP packages that perform the same function. As a result a compact package 10 may be achieved that has lower costs while substantially maintaining the form factor of corresponding (but more expensive) non-PSIP packages.

The passive components 16 may be selected to have a height not exceeding 16 mils in some embodiments. The vertical profile of this package 10 may be further reduced, in some embodiments, by the use of BGA packaging technology which has a relatively low vertical profile compare to the pin grid array (PGA) packaging technique. The x, y size of the package may be reduced by the use of attachment methods such as user-dispensed epoxy as the adhesive 18 rather than surface mounting the passive components 16 to the substrate 12 beside the die 14.

Referring to Figure 2, in another PSIP embodiment, a ball grid array (BGA) package 26 may include an integrated circuit die 29 mounted on a substrate 28. The upper surface of the substrate 28 may be encapsulated using an encapsulation 30 in one example. The package 26 is

electrically connected to external circuitry using a multiplicity of solder balls 34 disposed on the lower surface of the substrate 28. Passive components 32a and 32b including inductors and capacitors may form a charge pump located externally to and disposed beneath the die 29.

Referring to Figure 3, the components 32 may be attached under the substrate 28 within a central field 33 that may be free of solder balls 34. Subsequently the package 26 is attached to external circuitry by surface mounting the solder balls 34.

In one embodiment the height of the passive components 32a and 32b does not exceed the height of the solder balls 34. As a result the passive components 32 may be included on the lower surface of the BGA substrate 28 without increasing the height of the package 26 from what it would have been if the passive components 32 were integrated inside the die 29. Thus the package 26 has the advantage of a smaller die 29 size because of its PSIP design while it still has substantially the same form factor.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: